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Surface-emitting superluminescent LEDs

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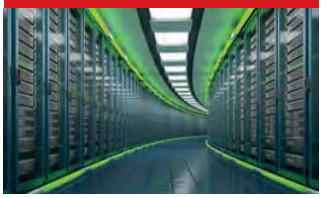

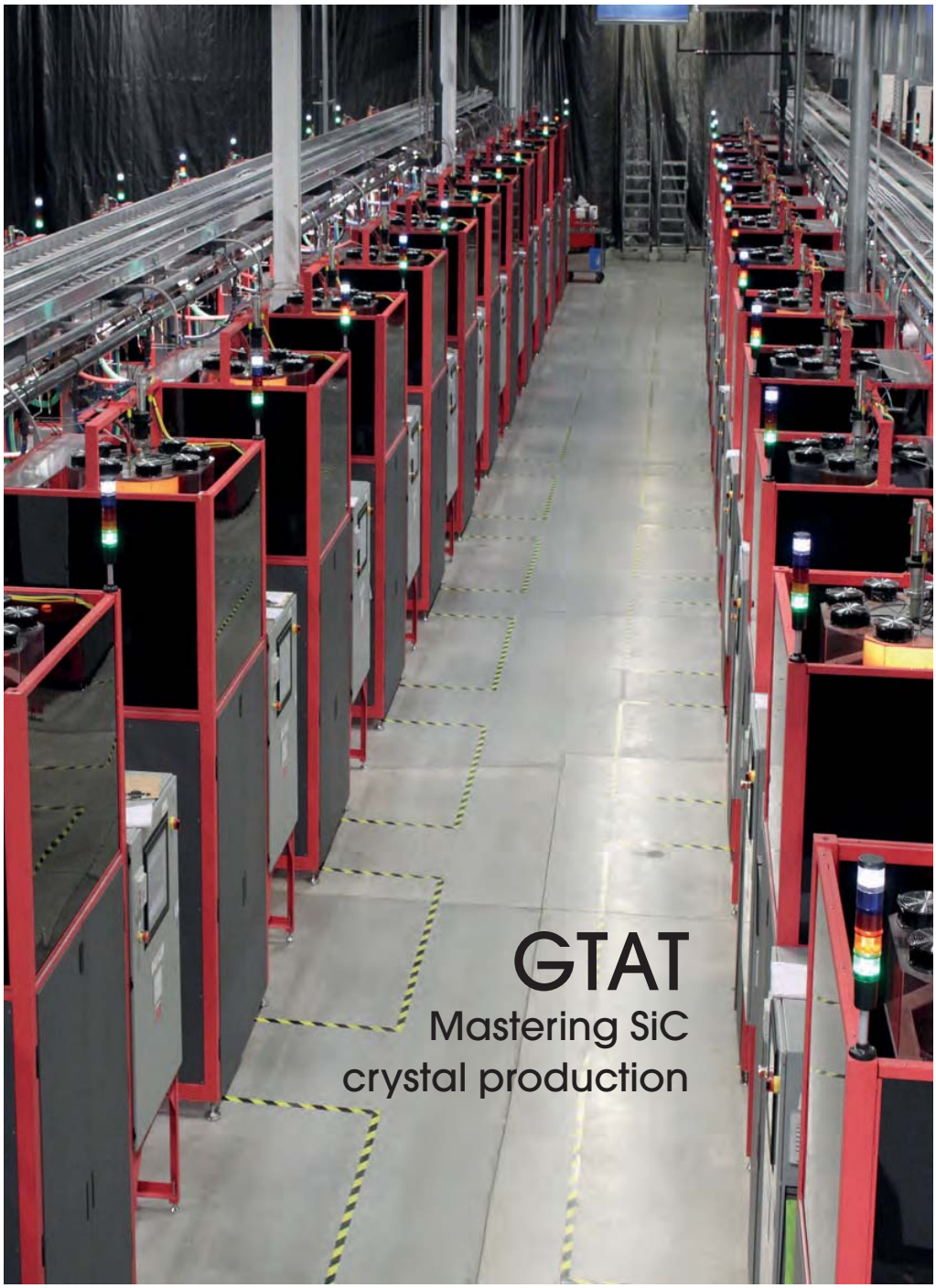

GTAT

Mastering SiC crystal production

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Opening up **SiC substrate** production

A manufacturer of crystal growth equipment pivots to materials manufacturing, creating a more competitive supply chain for the production of SiC power electronics

BY SANTHANARAGHAVAN PARTHASARATHY FROM GT ADVANCED TECHNOLOGIES

SILICON, the most widely used material across the entire electronics industry, has dominated power electronics for decades. But its vice-like grip is slipping. The silicon power devices used in all forms of power conversion – that includes AC-DC rectifiers, AC-AC transformers, DC-DC converters and DC-AC inverters – are struggling to keep up with demands for higher power ratings, faster switching frequencies and elevated operating temperatures. Failing to fulfil these requirements has undesirable implications, as circuits then need additional cooling and take up much more space, because they require large 'passive' components, such as inductors and capacitors.

Addressing all these weaknesses is a portfolio of materials with wider bandgaps, such as SiC. The wider bandgap is a wonderful attribute, delivering multiple benefits. For SiC, the bandgap is three times

that of silicon, providing a breakdown field ten times that of the incumbent (see table 1). Additional merits of SiC devices are efficient switching at far higher frequencies than silicon equivalents, enabling the use of far smaller passives, and a thermal conductivity three times better than silicon. Drawing on all these attributes allows SiC to hold the key to smaller, lighter circuits that are more efficient, handle higher voltages, and have reduced requirements for thermal management.

Such circuits are in growing demand as markets and applications push toward the 'electrification of everything'. Although this is most evident in the electric-vehicle industry, which is literally driving the transition from traditionally used silicon-based power electronics to SiC, other industries are also benefitting from this wide bandgap material. They include: power conversion systems featuring in other forms of transport, such as electrified trains, ships and aircraft; renewable energy applications, including solar photovoltaics and wind energy; and industrial/commercial applications, such as power supplies for servers, uninterruptible power supplies for data centres, motor drives and medical imaging systems.

In addition to all of these all-SiC devices, SiC provides the foundation to a variety of devices based on GaN. High-frequency GaN-on-SiC transistors are deployed in 5G telecommunication systems, such as repeater stations; and also in digital TV, radar and optoelectronic devices. In 5G applications, the combination of GaN epilayers and a semi-insulating SiC substrate creates devices that are superior to silicon LDMOS, and deliver increased capacity and coverage. Switching from silicon LDMOS to GaN-on-SiC doubles the number of users per tower and increases data transmission by more than an order of magnitude.

Substrate supply

As awareness of the superior properties of SiC grows, the demand for power electronics made from this material is ramping fast. Only a few companies are meeting this demand by growing high-quality SiC crystals, which begs the question: why aren't SiC crystals produced in volume?

The answer is multifaceted, and relates to the challenges of growing SiC. The wide bandgap material cannot be produced by the melt growth processes used to make boules of elemental semiconductors, such as silicon, which is manufactured by the Czochralski method. That's because a stochiometric melt is not realised under normal conditions. Instead of melting, SiC sublimes at about 2100 °C. For this reason, the growth of SiC requires a vapour-phase crystal growth process – generally a physical vapour transport or sublimation technique.

The fundamental crystal growth steps are essentially the same for vapour growth and melt growth. The process begins by generating reactants, either through sublimation or melting, and

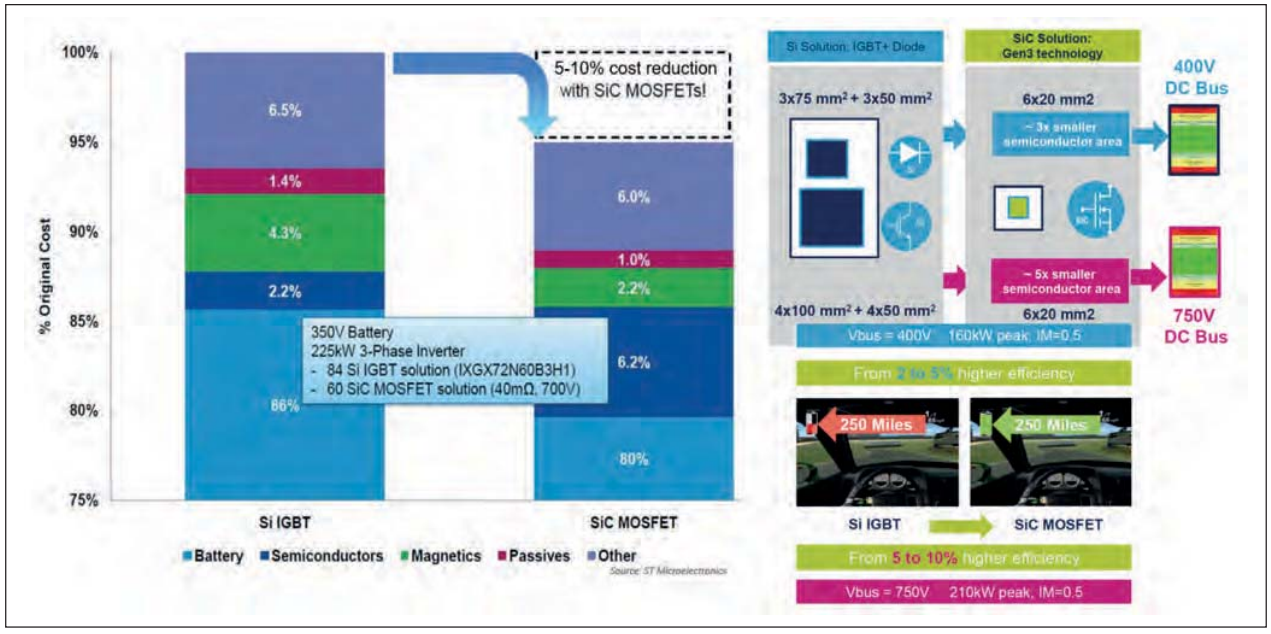

Figure 1. Switching from silicon to SiC offers savings at the system level. Source: ST Microelectronics

transporting them to the growth surface using specific temperature gradients. After this adsorption occurs at the growth surface – known as supersaturation – nucleation takes place, followed by crystal growth, which proceeds via either the advancement of the gas-solid interface or the solid-liquid interface.

Differences in the processes used for SiC and silicon boule growth are behind differences in the cost, size and availability of these substrates. For silicon, ingots produced in state-of-the-art crystal growth equipment have a diameter of 450 mm and a length exceeding 2 m, and are realised at a growth rate of around 100 mm/hour. Growth is initiated using a thin seed with a 10 mm by 10 mm cross section.

In contrast, SiC crystals are grown with a diameter of 150 mm, and have a length up to 50 mm, with growth proceeding far more slowly – it occurs at 100-300 μm/hour. This process begins with a starting seed that has a diameter of 150 mm or more and a thickness of 1-2 mm.

One significant barrier to entry for any company wanting to manufacture SiC substrates is that the high-quality starting seeds, which are needed to initiate the process, are not commercially available. Trying to get around this by using a commercial substrate as a seed for bulk crystal growth is not an option, as this is prohibited by SiC wafer manufacturers. Hence any new entrants to this market must spend considerable development time and resources generating high-quality seeds.

Like silicon, the SiC industry needs 'pure play' material suppliers. GT's supply chain strategy will enable this, opening up opportunities for existing silicon substrate providers to add SiC to their portfolios, leveraging established scale, mature value chains and established relationships with the IDMs who buy silicon substrates. Similarly, IDMs can rapidly add wafer capacity and increase their level of vertical integration.

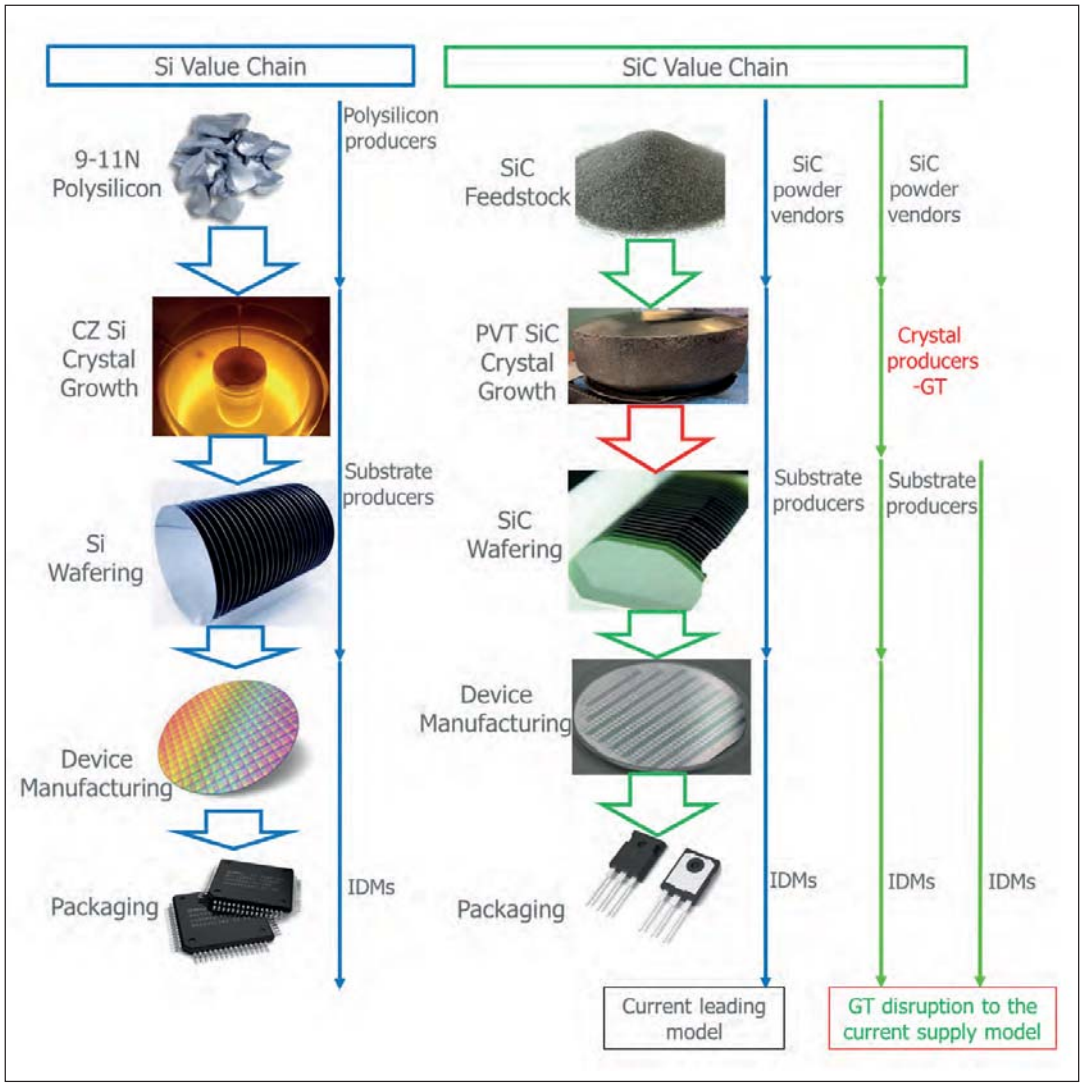

Figure 2. The SiC value chain has different challenges to that for silicon.

Along with slow growth rates and limitations to crystal size, difficulties associated with yield in the vapour growth process account for the far higher production costs of SiC crystals, compared with those made from silicon. Yet, despite the far higher substrate cost, even today a circuit designer that switches from using silicon devices to those made from SiC gets a 5-10 percent cost reduction at the system level. So the material already pays for itself, and its winning margin is only going to grow as the costs of SiC substrates and devices fall significantly over time. Note that in addition to the cost savings, SiC devices enable smaller, lighter systems, primarily due to their higher power densities (see Figure 1 for details of cost savings).

Another challenge associated with SiC relates to the many forms of this material. There are three crystal structures – cubic (3C), rhombohedral (15R) and hexagonal (2H, 4H, 6H, etc.) – and the number of polytypes exceeds 200. The 4H polytype of SiC, used for power electronics, accounts for around 60 percent of the SiC market. Devices are made on *n*-type SiC, produced by doping with nitrogen gas. This results in a resistivity in the 0.015 to 0.025 Ω cm range – it is typically 0.020-0.022 Ω cm. Sales of substrates for making RF devices account for 40 percent of the SiC market. These devices involve the growth of GaN-based heterostructures on 4H semi-insulating substrates. Produced by either doping with vanadium, or the absence of doping, they have a resistivity exceeding 10,000 Ω cm. For opto electronic device application, 6H polytype is used.

The quality of SiC lags that of silicon. The latter can be grown free of defects, while SiC suffers from fundamental issues associated with vapour-phase growth, multiple polytypes and a spiral growth mechanism. Part of the problem is that the stacking fault energy needed for the atoms to migrate to, and sit in, the right place is far lower in SiC than silicon. This introduces a wide range of defects,

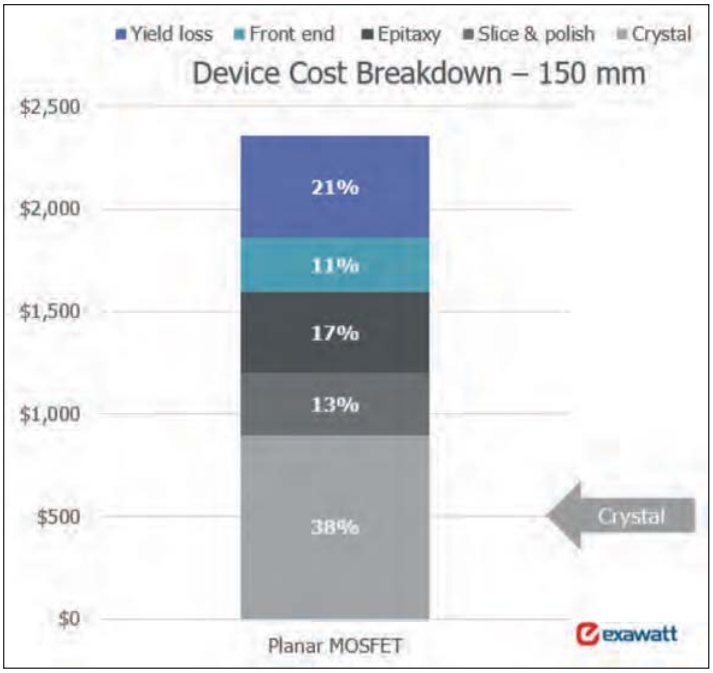

Figure 3. The cost breakdown for a SiC MOSFET produced on a 150 mm wafer. Source: Exawatt

including micropipes, carbon inclusions, and extended crystal defects, such as threading screw dislocations, threading edge dislocations, basal planar defects and stacking faults. Mitigating these defects is not easy, requiring a combination of equipment expertise and process knowhow. Just one without the other is insufficient for delivering the results demanded by high-growth markets.

Accelerating cost parity

At GT Advanced Technologies, also known as GT, we have developed and refined a high-yielding crystal growth process for large-volume, low-cost SiC boule production. This is helping us meet our primary objectives of accelerating cost parity between silicon and SiC, and greatly increasing the supply of this high-demand material.

Our efforts have enabled us to produce 150 mm diameter SiC substrates using mainstream production processes. As the availability of larger-diameter wafers is key to lowering device cost and improving die yields, we have also started development work on 200 mm boules.

The price of the SiC substrate is governed by the costs associated with the furnace architecture and infrastructure – factors such as the cooling water supply, the cost and need for uninterruptible power, the space occupied, the exhaust system and HVAC. There are two options for creating the high temperatures needed for SiC sublimation: a resistively heated furnace, with heat transferred from the heater to the crucible by radiation; and inductive heating of the crucible, which acts as the heater. One downside of resistive furnaces is a high fixed cost profile, stemming from equipment capex, the large footprint and infrastructure. Using this form of heating, there is limited opportunity to trim costs through operational and technical improvements. The promise of savings is far greater with inductive platforms. They offer a much lower fixed cost burden, due to lower capex, higher productivity, a lower electrical consumption, and a smaller footprint.

By adopting the inductive approach for reasons just outlined, we have positioned ourselves as a cost leader today, with a tremendous headroom for further improvements. Our production process enables high yields, high-quality and low cost, thanks to extensive thermal modelling skills, combined with excelled equipment design and process control innovations. The boules we produce have low defects, both for micropipes and other crystalline defects, and are manufactured in a cost-effective manner, due to a very high run-to-run reproducibility.

We are also able to draw on established supply-chain resources, equipment design and build capabilities, and process expertise. These strengths put us in a great position to scale quickly with demand and further improve our production processes over time. This will steadily increase our competitiveness in providing a low-cost, high-volume supply of SiC bulk materials.

The challenges of SiC substrate production are not limited to crystal growth. Processing boules into wafers is not easy, due to in-built thermal stresses arising from the growth process and a high material hardness – it is second only to diamond. Substrate production begins by grinding the SiC crystal to a specific diameter and then undertaking multi-wire sawing, using either a diamond slurry, a diamond-fixed abrasive wire, or laser-based wafering. This is followed by coarse and fine grinding of the surface, edge grinding and chemical-mechanical polishing.

Device makers will take the epi-ready substrates, load them into an MOCVD chamber, heat this to 1600 °C, and grow an epilayer using propane as the source of carbon and silane or trichlorosilane as the source for silicon. Depending upon the intended device breakdown voltage, the thickness of this drift layer will be somewhere between 5 μm and 100 μm (the drift layer thickness is approximately 1 μm per 100V, so for a 11 kV device, the epilayer thickness needs to exceed 100 μm).

To realise excellent reliability and drive improvements in yield and cost, device production may draw on recent refinements, such as gate oxide and thermal oxidation processes. Such techniques have helped expand the portfolio of SiC devices, which include Schottky barrier diodes, MOSFETs, HEMTs, MesFETs, JFETs, cascodes and BJTs, with operating voltages spanning 600 V to 30 kV. Power modules have also been produced from SiC devices, using developments

	Ge	Si	GaAs	4H SiC	4H SiC comments
Bandgap (eV)	0.67	1.1	1.4	3.3	Larger bandgap, lower leakage current, higher operating temperature and radiation resistance
Breakdown field E_c (MV/cm)	0.1	0.3	0.4	2.5	Higher breakdown field, lower on-resistance and higher blocking voltage
Thermal conductivity W cm^{-1} C^{-1}	0.58	1.3	0.55	3.7	Higher thermal conductivity, which increases heat spreading and power density
Relative dielectric constant ε	16	11.8	12.9	9.7	Lower dielectric constant – less parasitics
Electron velocity υ_s (cm/s) x 10^7	0.6	0.9	1	1.5	High electron saturation drift velocity leads to smaller devices
Electron mobility μ (cm^2Vs^{-1})	3900	1400	8000	1000	
Johnson Figure of Merit (Maximize Frequency and Voltage)	1	5	7	63	
Baliga Figure of Merit (Minimize conduction losses)	1	7	106	2429	

Table 1. Physical properties of germanium, silicon, GaAs and SiC.

in packaging technology, such as direct-bonded copper and direct-bonded aluminium-on-AlN. These modules can operate at temperatures beyond 200 °C.

The supply chain for SiC power electronics is markedly different from that for silicon (Figure 2). The former is held back by the limited availability of SiC crystal, a major bottleneck that we are eliminating through our supply chain strategy. In comparison, integrated device manufacturers (IDMs) in the silicon industry are buying material from multiple substrate producers. Complicating matters, the leading incumbent SiC substrate vendors also make their own devices, so they compete against their downstream customers.

Like silicon, the SiC industry needs 'pure play' material suppliers. GT's supply chain strategy will enable this, opening up opportunities for existing silicon substrate providers to add SiC to their portfolios, leveraging established scale, mature value chains and established relationships with the IDMs who buy silicon substrates. Similarly, IDMs can rapidly add wafer capacity and increase their level of vertical integration. In either case, costs should rapidly decline as scale is added and industry freed from its dependency on just a few merchant suppliers.

This transformation of the SiC industry will deliver much success in the power electronic industry. Today, a single epi-ready 150 mm SiC substrate retails for $800-$1,100, accounting for a significant proportion of the device cost (the cost breakdown of a MOSFET is given in Figure 3). The cost of this substrate can tumble – we expect it to fall to just $300 in the years to come. One of the keys to this price reduction is increasing the useable height of the grown crystal, as run costs are relatively independent of crystal height.

Additional drivers are lowering capex, reducing operating costs, increasing productivity, tightening process control and increasing factory yield – crystal growth yield must be pushed above 98 percent, while crystal fabrication yields needs to go beyond 95 percent.

Our expertise in SiC crystal growth has led us to make the strategic decision to focus solely on this, drawing on our knowledge and experience in crystal growth equipment and SiC growth. We are offering the world's wafer producers a large supply of high-quality SiC crystal. This offering broadens and deepens the global supply of SiC wafers, helping drive down costs.

The power device industry is already welcoming these market developments. Illustrating this, in August 2019 GTAT signed a long-term agreement with GlobalWafers to supply its CrystX SiC crystal, and in early 2020 signed a long-term supply agreement with ON Semiconductor, one of the leading IDMs.